Stanley A Meyer Hydrogen On Demand
Analysis and Test Results of Resonant Scanning Circuit K22

The main purpose of this circuit is to create a voltage control pulse train that is used to find the resonant frequency of the cell. A clock wave train is generated locally in A31, a 555 timer, this pulse train is modified in A32 to create a double ramp voltage control pulse train, ramps on leading and trailing edges, that is sent to the Phase Lock Circuit K21 as signal (F). This part of the process never stops. However, when K21 determines the system is in resonant its sends K22 a high signal on interface (L). When this happens the Lock signal (L) is used to change the output from the local generated control pulse train to the resonant frequency that is receives from K21 as signal (E). Signal (E) is routed back to K21 as signal

(F) and frequency scanning stops. When K21 senses that the systems has dropped out of resonance it sends an unlock low signal on (L) which causes output on (F) to be switched back to the voltage control scanning pulse train generated by K22.

This process keeps repeating the only thing that changes it is the manual-auto switch on the front panel. In manual mode the 50K POT on the front panel generates a voltage level. This voltage level is used by the Voltage Controlled Oscillator (VCO) in K21 to determine what frequency to output.

Inputs

1. VCC +12 VDC
2. Ground 0 VDC
3. +10 VDC- from 10VDC regulator (needed by A32 LM741)
4. Front Panel – Manual / Auto Switch (ON-ON)
5. Front Panel- 50K Pot
6. Signal (L) – Lock signal from K21 (high/low)
7. Signal (E) – Resonant Frequency from K21

Outputs

1. Signal (F) – with voltage control pulse train required to drive VCO
    a. Auto Mode
        i. Double ramp pulse train when not locked
        ii. Signal (E) when locked
    b. Manual Mode
        i. Voltage level from POT

Circuit Analysis

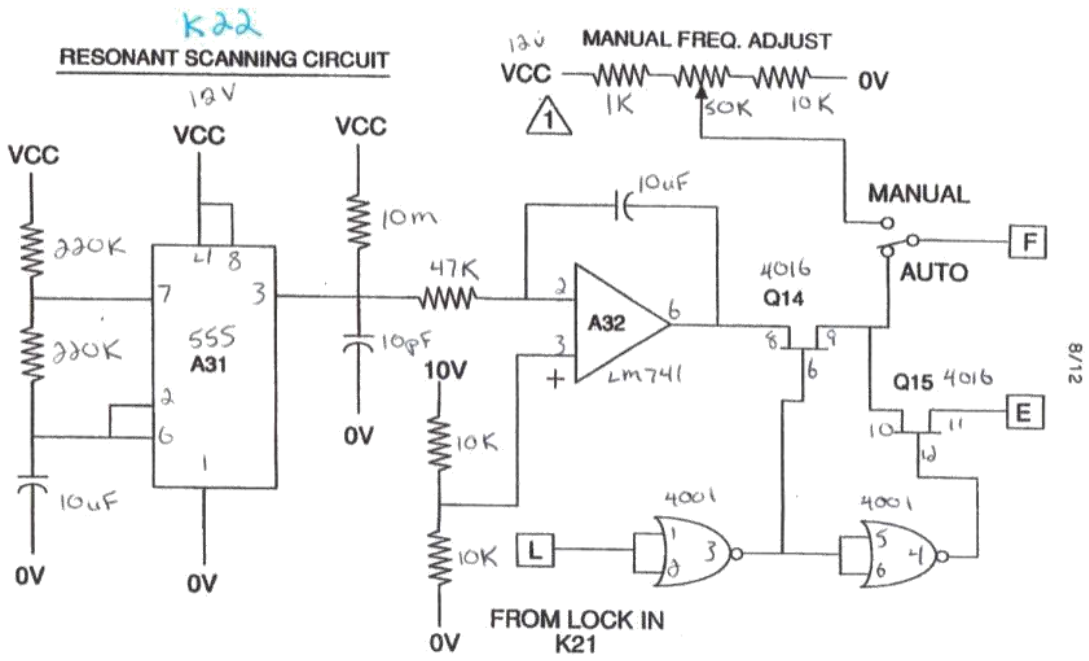

FIGURE 8

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The resistors and capacitor around A31 and A32 are used to set the devices in the desired operational mode. For A31, 555 Timer, the set it in to generate a clock pulse at frequency set by the bias resistors and capacitor. This pulse train is sent to A32, 741 Opamp, set up in voltage follower mode. It generates a double ramp 10-volt pulse out of each clock pulse. By double ramp I mean there is a ramp up on leading edge and ramp down on training edge. The slope of the ramps is set by the capacitor on feedback loop from pin 6 to pin 2.

> NOTE: 12-volt VCC determines range of output signal as rails of device are 2-volts from max/min values. 10-volt source on input 3 along with resisters sets its input voltage to 5-volts.

The Lock signal (L) from K21 sets the states of the 4001 logic devices and the states of the Q14 and Q15, switches, this determines which signal is routed to output (F) the local pulse train when scanning or the resonant frequency (E) from K21 when system is in resonance.

In Manual mode the 50K POT with the bias resistors can be used to set the center range of the VCO in K22. The POT can also be used to manual set the operational frequency to a desired value.

> NOTE: I have already done some preliminary testing of K21 and built a similar POT as a separate circuit to help me understand the operation of the VCO and select values to set center range. Once I finish testing this circuit, I will be using manual mode to do final testing of K21.

Test Procedure

I will be testing this circuit initial as a standalone circuit. Purpose is to verify circuit is functional and to determine ranges of outputs based on the valves identified on circuit drawing. I will do interface testing with this circuit and K21 later and report that testing in the tests of K21.

Because of this I will be creating alternate means of generating signals (L) and (E).

Test Configuration

I will be using an LM317 card I purchase that has all the support chips on it to generate the 10VDC supply for A32 needed on input 3.

Variable Frequency Generator (Board K2) hard wired and tested version. Initial plan is use K2 as a frequency source for (E) just to verify path to (F) functions when system is in lock mode.

Note: This was my plan before I started testing but I did not do this. I used output of A32 instead and a jumper to connect it to input (E).

12VDC (VCC in circuit) will be provided from a 12-volt switching power supply as I had a couple from old computer equipment.

RIGOL DS1052E – Duel Channel Digital Oscilloscope will be used to capture the wave train. Screen shots of signals at various locations through the circuit will included in test results. Scope's computer interface will be used to capture screen shots as will the clip-it function in window to get information into this document.

Digital Voltmeter – So I can see voltage changes from POT, I can see actual values instead of level on scope. I also displayed voltage on O-Scope so it in screen shots.

Check Manual Mode

I know what to expect from this output so I am going to start here will record minimum and maximum values. Note: Values will reflect values of POT I am using I have found them to be slightly less that 50K but should be close enough to get a feel or correct ranges. I have also found in Stan's circuits that they are never used near limits. Again, these voltage levels will be used by VCO to generate 50% digital pulse with frequency based on voltage level.

Capture Voltage Level out of Pot at Max Setting

CH1 – Yellow Scale 5V/Div

Vmax(1) – Max value of signal

Vmin(1) – Min value of signal

Signal is a flat line and reads 12.14 on Voltmeter

Capture Voltage Level out of Pot at Min Setting

CH1 – Yellow Scale 5V/Div

Vmax(1) – Max value of signal

Vmin(1) – Min value of signal

Signal is a flat line and reads 2.21 on Voltmeter

Capture Voltage Level out of Pot at Mid Setting

CH1 – Yellow Scale 5V/Div

Vmax(1) – Max value of signal

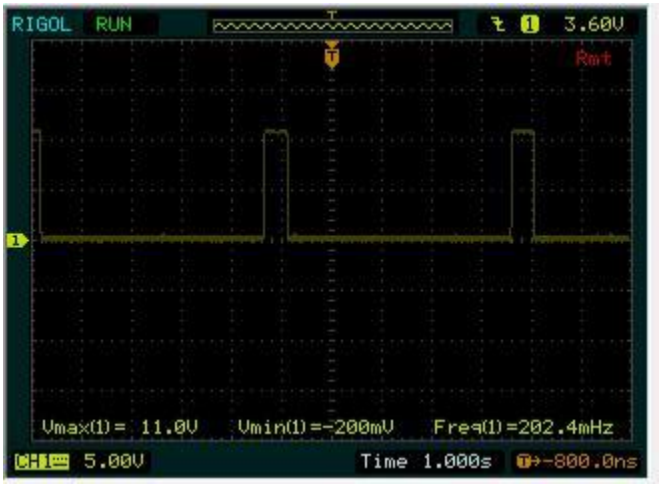
Vmin(1) – Min value of signal

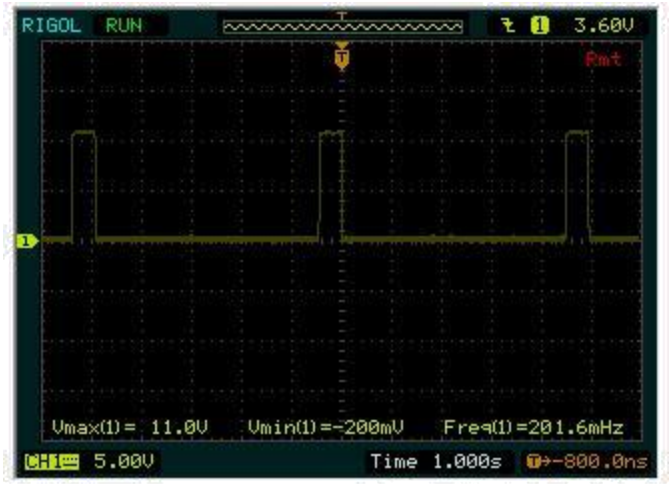
Signal is a flat line and reads 7.42 on Voltmeter

Change Switch to Auto Mode

CH1 – Yellow Scale 5V/Div

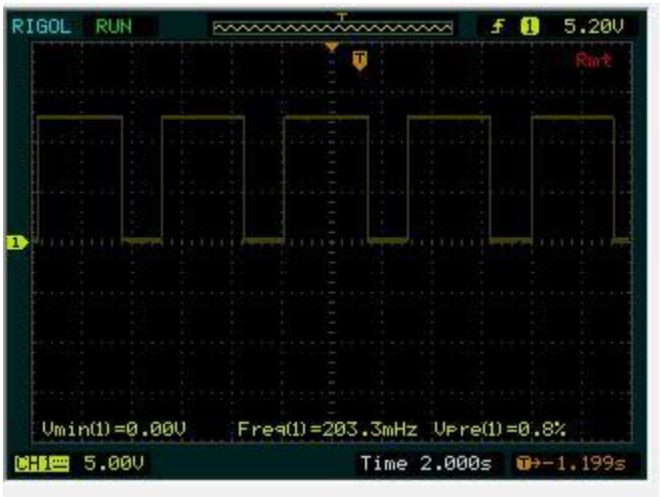
Signal changes to very slow pulse at 11-volts peak





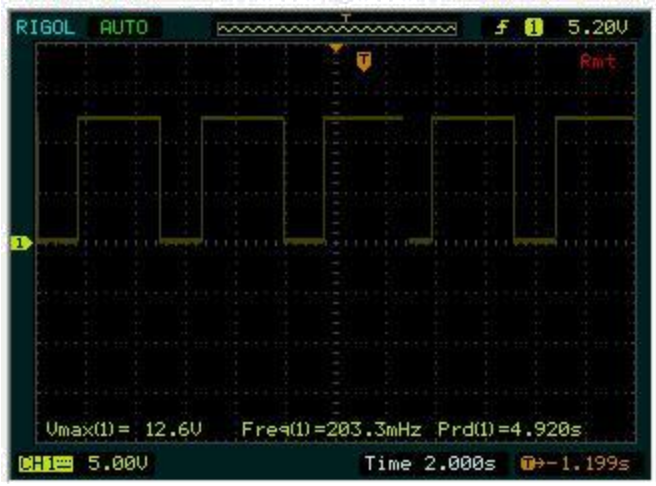
Capture output of A31 Pin 3 before 47K Resistor

CH1 – Yellow Scale 5V/Div



Screen below show screen being redrawn

CH1 – Yellow Scale 5V/Div

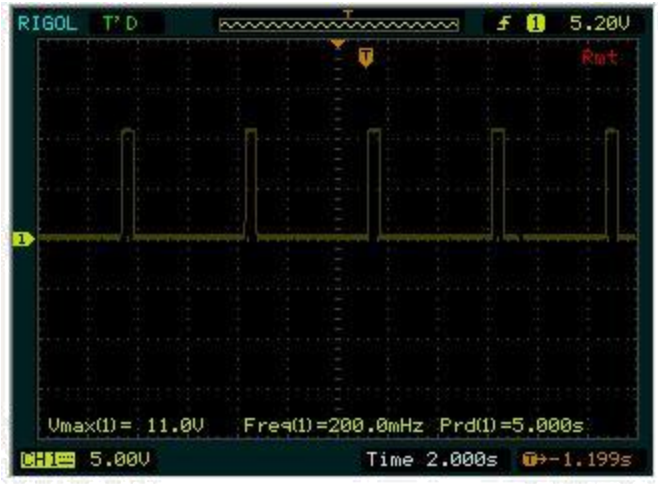


Capture input to Pin 2 of A32 after 47K resister

CH1 – Yellow Scale 5V/Div

No change to scope setting

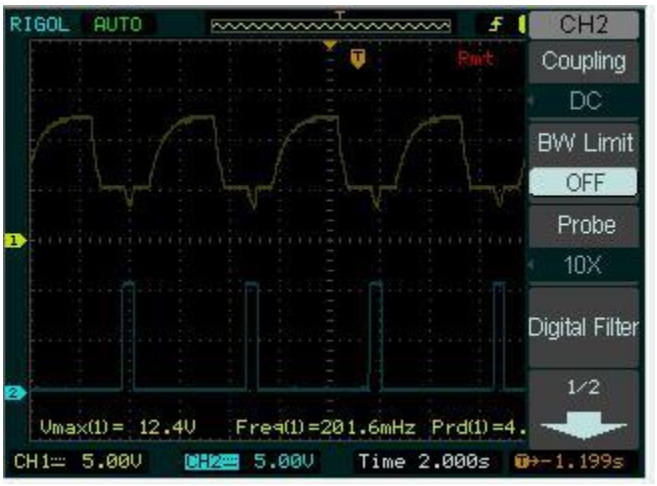
Capture output (F) at this point



Capture input to A32 pin 2 and output (F) at same time

CH1 Yellow Pin2

CH2 Blue output (F)

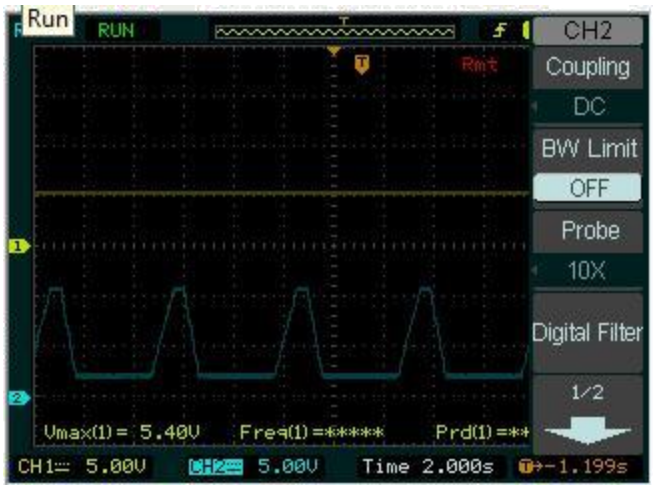


Capture input to A32 pin 3 and output (F) at same time

CH1 Yellow Pin2

CH2 Blue output (F)

Shows input on pin 3 to be a constant 5.4-volts as would be expected using resister divider across 10-volt source.

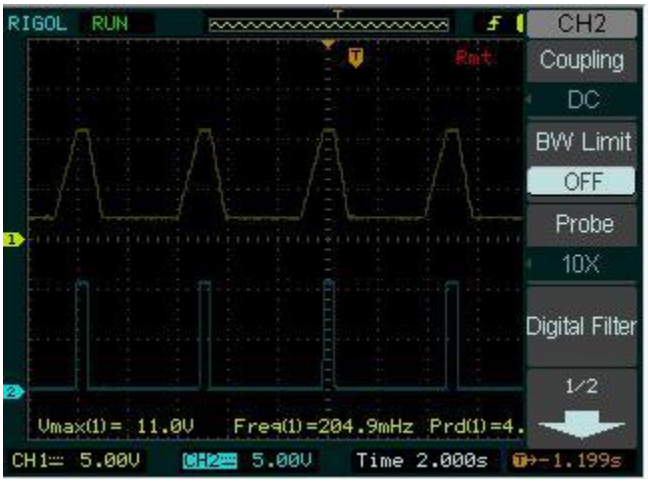


Capture input to A32 pin 6 out and output (F) at same time

CH1 Yellow output (F)

CH2 Blue pin 2

Note: Scope probes switched here



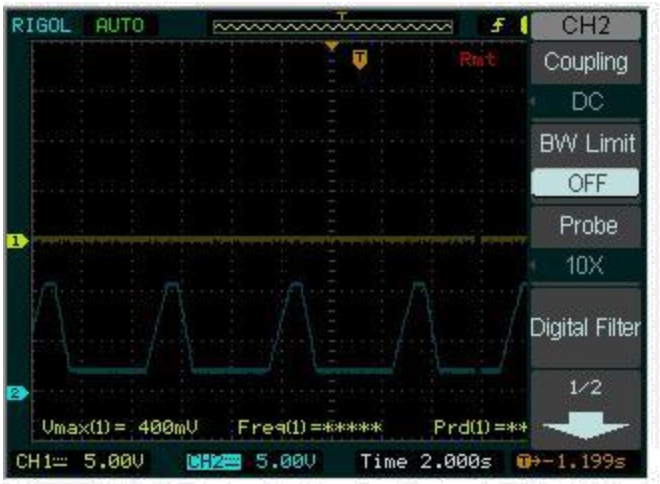
Check input (L) on pin 1&2 of 4001

CH1 Yellow Pin2

CH2 Blue output (F)

At zero as expect as current no connect to (L) but does tells low signal is no Lock as sign is getting out on (F)

Scope probes switch back to blue on output side

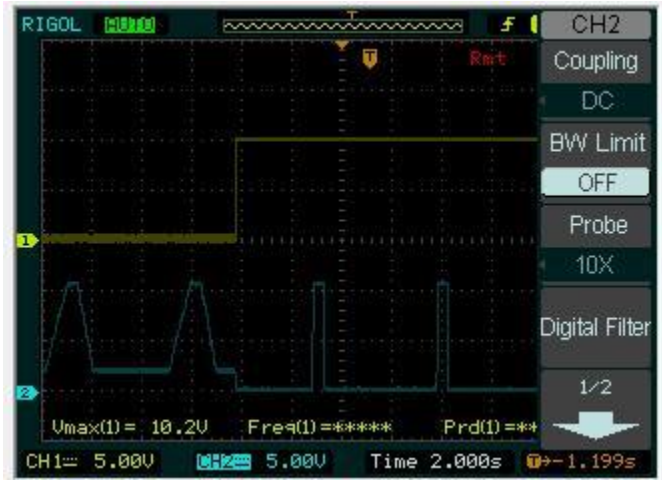


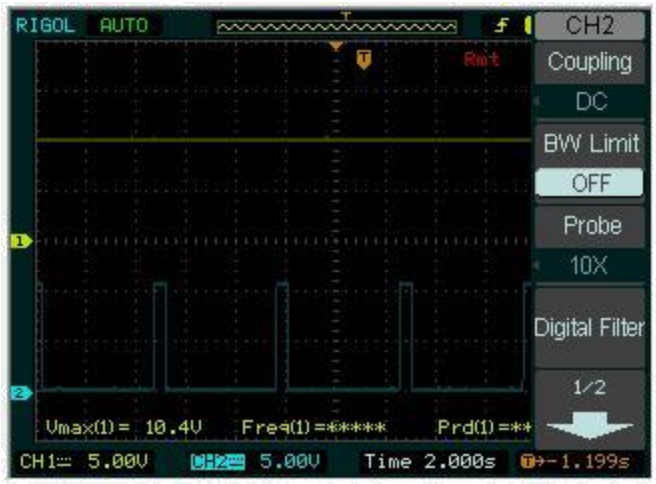
Capture input (L) set manual at +10-volts and output (F) no input on (E)

CH1 Yellow Pin2 Manual set to 10-volts to trigger Lock

CH2 Blue output (F)

You can see the output sign change in next screen and one after that is after it settles out



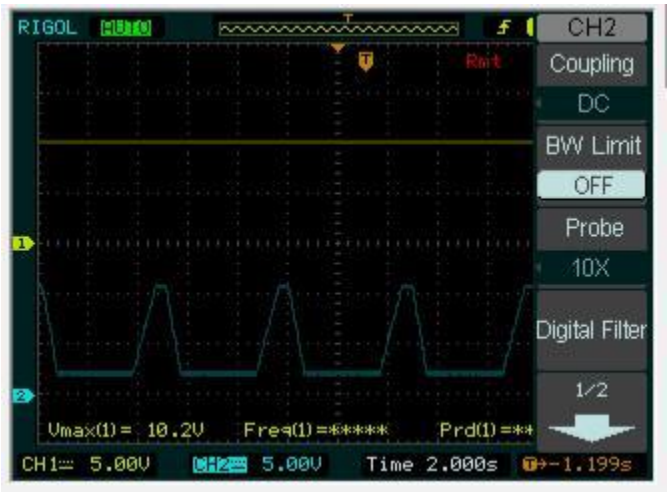


Capture A32 output pin 6 connected to (E) input while Lock is set

Output of A32 pin 6 was connected to Input (E) to provide an input to flow back out to (F)

CH 1 show that normal path is blocked as Lock indicator is set high

So this show alternate path works and new input is through the (E) signal input showing this part of the circuit works NOTE: This is not the normal input but it does show this function does work in this circuit as in this mode it is just a throughput path back to K21.

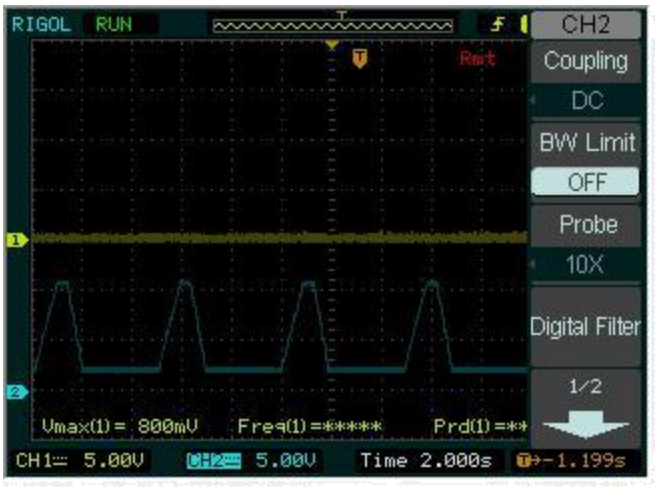


I removed (E) then (L) and signal returned to normal mode.

Capture (F) and (L) to show normal Auto mode with No Lock

CH1 Yellow Pin2 No Lock

CH2 Blue output (F)



This completes this phase of testing. While I will do a quick check to verify everything is still working after I transfer components to hardwired version, I am satisfied the board is working properly and now have a record of what it does.

Future testing will be with the Phase Lock board K21 to verify interfaces between boards functions correctly. As the (F) signal from this board K22 is needed by K21 I will be using it during testing of that board now that I have verified this board is function correctly.

Note: When I testes the final card everything worked except way train was not right out of 4016 IC I spent and 1.5 hours checking things. Then hooked up a ground wire to Latch input which fixed problem. Had tried it earlier but must had a bad connection. Looks like 4016 does not like floating input. I this case I had left ground off as it is not part of this circuit.

Test Results and Conclusions

Testing Results of Manual Pot

Range from voltmeter is 2.21-12.4 volts. Taken on (F) output.

Manual setting on switch provides POT output.

Pot works as expected and so does selection switch,

Auto Mode Testing

The Lock signal (L) functions in circuit

Unlocked mode – Signal level is **Low** and the ramped pulse flows out as signal (F)

Locked mode - Signal level Is **High**

No signal (E) - sharp pulse with no ramps flows out as signal (F)

Signal (E) present - Signal is sent out on signal (F)

Scanning Signal Generation

A31, 555 Timer, generates a clock pulse as expected but it is not as fast as I expected after building and testing K2. My expectation was it going to create multiple frequencies, which is not the case. Instead, as can be seen from the scope shots it creates a slow 12-volt pulse train that is passed to A32. A32 takes this input and turns it into a 10-volt double ramped pulse train that is the normal output (F) signal when the system is the unlocked scanning mode.

Why a double ramped pulse (ramp on both rising and falling edges). This circuit does not actually generate the frequencies the Voltage Controlled Oscillator (VCO) in K21 does that. Th VCO uses the ramp voltages generated here to generate the scanning frequency necessary to scan across the frequency range set in the CD4046B. So, the frequencies are scanned one direct across the range, there is a small pause then frequency are scanned back the other direction. There is a longer pause then cycles repeats until lock it found. That pauses are set here by the resistors and capacitor around A31.

Final Conclusion

I believe this circuit is functioning as designed. However, I will also state that without some understanding of what K21 is doing this circuit would not have made sense to me. It helped that I started testing K21 before I started testing this circuit. A ran into a couple of issues with K21 that led me to dig deeper in the what the CD4046 is doing. One of the things I found is I could not get any output from it to drive the signal dividers. As that signal comes from the VCO I looked closer at it, and found I needed a voltage input to generate that signal which I was missing. That missing signal was (F) by then I also knew it need to be signal at different voltage levels. I expected a pulse train where level of the pulses changed. Instead I got the ramped pulses, so I was partly right. The ramps made sense after I saw them and thought about what happens to them downstream, they generate the scanning frequencies both up and down as the voltage is changing when the ramp is present.

The manual mode does the same thing but without the ramps and does it slower. It allows the operator to look at selected frequencies for a long time if desired. It also is another tool as it can be used to adjust the center point for the scanning POT which is affected by the voltage level on Pin 9, where signal (F) is connected.

Building and testing this circuit met my goals. I now know what it does and why. I also now know what the signals coming out of it look like and what their levels are. Please note. This circuit does set the scanning range that is done in K21. This circuit just setup the conditions to scan across that whole range though by angle of ramp it does set speed of scan. If you want to change that you will need to adjust the bias resistors and capacitors in this circuit.