

between 143 kHz and 200 kHz and the duty cycle defaults to approximately 1.3% on.” The article does not include any oscilloscope captures that might be used to communicate actual circuit performance as experienced by the authors.

Here we deal only with the performance of the documented circuit. Unfortunately, the article includes some contradictory information as to the actual circuit construction. The article includes a bill of materials with reference designators. The schematic diagram does not include reference designators. A minor discrepancy is that the schematic calls for a 5.2K resistor which is not a standard 5% value, while the bill of material calls for a 5.1K resistor, which is a standard 5% value. The 100 Ohm difference is insignificant to the operation of the circuit, and we assume that the bill of material value is correct and that the schematic value is a typographic error.

A more serious conflict that arises is the call-out of a 0.0033uF (3.3nF) capacitor in the schematic, but 33nF appears in the bill of materials. The bill of material includes distributor product codes. The product codes no longer appear to be valid preventing determination whether the capacitor is 3.3nF as shown in the schematic, or 33nF as shown in the bill of material. This author evaluated actual circuit performance using both values. This author finds that neither circuit variation is capable of generating the claimed 3.7% on duty-cycle stated in the article at any combination of the potentiometer settings.

<i>Schedule of components</i>		
Parts list for experiment		
	Value	Farnell code
R1	50K Pot 10 turn	351-817
R2	50K Pot 10 turn	351-817
R3	1 K.25w	509-164
R4	1 K.25w	509-164
R5	5K1.25W	509-164
Preset	100R	614-622
Load	10R	*As per description
Shunt	1R2W x4	Connected in parallel
Caps		
C1	100µF/16V	228-503
C2	10nF	579-129
C3	33nF	579-154
C4	47nF	579-166
Semiconductors		
D1	1N4007	365-282
D2	1N4148	368-118
D3	1N4148	368-118
U1	NE555	409-364
Q1	IRFPG50	355-744
Batteries		
B1	12V	174-804
B2	24V 2x12V 20ah	Battery Centre

Figure 2, Bill of Material from ‘Quantum’ Article

For purposes of convenience in discussion and comparison we present a redrawn version of the schematic that properly labels the 555 pins and assigns reference designators, and which follows normal left to right signal flow convention. The schematic with the BOM based values appears in Figure 4.

LM555 Theory of Operation

The LM555 is a versatile device that consists of: Two input voltage comparators, Trigger and Threshold, a resistor divider, a Control Voltage input, an RS latch with a Reset input, an output buffer, and a Discharge open collector transistor. The output signal is high when the RS latch is set, and low when the RS latch is reset.

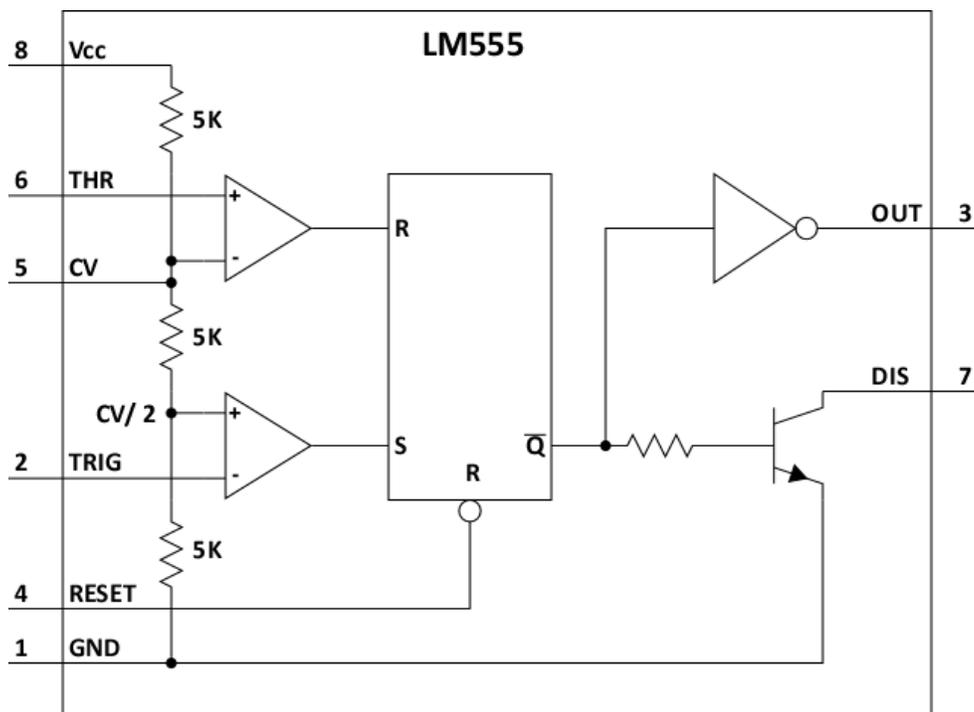


Figure 3, LM555 SIMPLIFIED CIRCUIT

When less than 0.4V, the Reset input: Pin 4, resets the RS latch independent of the comparator states. When more than 1.0V, the Reset input is inactive and the comparators control the RS latch.

Voltage at the Threshold input: Pin 6, above the control voltage input: Pin 5, resets the RS latch. Once the latch is reset the Output: Pin 3, switches and remains low, and the open collector Discharge output: Pin 7, presents low impedance to ground. Pin 7 typically discharges an R-C timing network connected to Threshold: Pin 6.

Voltage at the Trigger input: Pin 2, less than half the Control Voltage input: Pin 5, while the Reset input: Pin 4 is greater than 1.0V sets the RS latch. Once the latch is set the

Output: Pin 3, switches and remains high, and the open collector Discharge output: Pin 7, presents high impedance.

The time that the output signal of a 555 is high is the time it takes from the when the voltage at the Trigger input: Pin 2 rises above Control Voltage: Pin 5 * 0.5 to when the voltage at the Threshold input: Pin 6 rises above Control Voltage: Pin 5. The time that the output signal is low is the time it takes for the voltage at Threshold input: Pin 6 to fall below Control Voltage: Pin 5 until the voltage at the Trigger input Pin 2 falls below Control Voltage Pin 5 * 0.5.

The internal resistor divider consists of three equal value resistors connected in series from: Vcc to Control Voltage Pin 5 to the trigger comparator and then to ground. If no external DC connection is made to Pin 5, then the threshold comparator switches state at $V_{cc} * 2/3$ and the trigger comparator at $V_{cc} * 1/3$. Because the comparator thresholds are proportional to the Vcc supply, 555 resistor / capacitor timing networks charged from Vcc and discharged through the Pin 7 Discharge pin are very immune to Vcc supply voltage variations.

‘Quantum’ Magazine 555 Circuit Theory of Operation

The circuit presented in the October 2002 ‘Quantum’ Magazine article ties the Reset input to the Vcc pin, disabling reset operation. The circuit ties the Threshold Pin 6 and Trigger Pin 2 together to a timing capacitor C3 and two resistor networks connected through steering diodes D2 and D3: One network charges capacitors C4 and C3 during on times through D2: R5, R1 and, R3, and another network discharges C3 during off times: R2 and R4, while the LM555 discharge pin discharges C4 at the start of each off interval.

Compared to a typical LM555 astable circuit, the additional timing capacitor C4 asymmetrically extends on time and off times. C4 charges through the series combination of R5 and R1 during on times, and discharges through the Pin 7 open collector transistor during off times. The effective resistance of Pin 7 Discharge during RS latch off times is much less than 100 Ohms. The minimum value of the R5 and R1 combination is the value of R5: 5.1K Ohms. This is many times larger than the effective resistance of the discharge transistor resulting in on time extensions due to C4 that are much greater than the off time extensions due to C4. Absent C4, possible on time and off time ratios would range over the possible ratios of the series combination of R5, R1, and R3 to the series combination of R2 and R4. The incorporation of C4 by the circuit designer skews those ratios towards longer on times and therefore higher duty-cycles. The two steering diodes: D2 and D3 introduce small supply voltage sensitivity to on and off period timing. A well regulated 12V supply should be used to minimize the effects of the added sensitivity.

Because of the steering diodes: D2 and D3, there is very little interaction between on time adjusted by R1 and off time adjusted by R2. Larger R1 values result in: Longer on times, higher duty cycles, and lower frequencies. Larger R2 values result in: longer off times, smaller duty cycles, and lower frequencies.

Table 1, 'Quantum' 10/2002 Circuit Timing vs. Pot Settings

R1	R2	On Time	Off Time	Duty Cycle	Frequency
Zero	Max	Minimum	Maximum	Smallest	Intermediate
Max	Max	Maximum	Maximum	Second smallest	Lowest
Ctr	Ctr	Intermediate	Intermediate	Intermediate	Intermediate
Zero	Zero	Minimum	Minimum	Second highest	Highest
Max	Zero	Maximum	Minimum	Highest	Low

Experimental Measurement of the Published Circuits

In order to resolve the likely true circuit used by the authors, this author constructed both variations of the published circuit:

Configuration A: C3 with the schematic value 3.3nF, C4 47nF

Configuration B: BOM values for components. C3 33nF, C4 47nF

This author connected the test circuit to an Agilent E3846A bench power supply set to 12.0V. This author omitted D1 from the circuit.¹ This author then ran tests with the variable resistors R1 and R2 at their four extreme value combinations. The four corner values yield the following results independent of absolute circuit values:

¹ The only effect of D1 is to reduce the effective supply voltage to the circuit. Timing sensitivity at 11.3V versus 12V is found to be only a few percent.

Table 2, Timing Measurements of the Published Circuit

Configuration A, from Schematic C3 = 3.3nF					
R1	R2	On Time us	Off Time us	Duty Cycle	Frequency kHz
Zero	50K	303	116	72.3%	2.384
50K	50K	3206	116	96.5%	0.301
Center	Center	563	13.4	97.7%	1.734
Zero	Zero	301	2.9	99.1%	3.292
50K	Zero	3180	2.9	99.9%	0.314
Configuration B, from BOM C3 = 33nF					
R1	R2	On Time us	Off Time us	Duty Cycle	Frequency kHz
Zero	50K	467	1307	26.3%	0.564
50K	50K	4711	1305	78.3%	0.166
Center	Center	849	146	85.3%	1.006
Zero	Zero	471	27.3	94.5%	2.006
50K	Zero	4729	27.5	99.4%	0.210

Figure 5 shows oscilloscope captures for Configuration A, while Figure 6 shows oscilloscope captures for Configuration B.

Published Circuit Experiment Results Discussion

Configuration B using the published bill of material value for C3: 33nF is unable to reach 2.4kHz at any combination of R1 and R2 settings, whereas Configuration A easily reaches that operating frequency. This author concludes that the likely circuit configuration was therefore with C3 as documented in the schematic diagram and that the bill of materials is in error.

No combination of R1 or R2 values in Configuration A yields a duty cycle less than 72.3%. This creates a puzzle as to if the authors obtained a 3.7% on duty cycle as they stated, and if they did how they managed to do so with a circuit similar to the one they presented. A 2.4kHz 3.7% on duty cycle circuit translates into an on time of 15.4us, and an off time of 401.3us. The on time runs from when C3 falls below CV/2, also Vcc/3 until C3 charges to CV, also Vcc * 2/3. A first approximation of this time interval is:

Equation 1²: On time $\approx 1.17 * ((R5 + R1 + R3) * C3 + (R5 + R1) * C4)$

Equation 2: Off time $\approx 0.69 * (R2 + R4) * C3$

The sum R2 + R4 can range from 1K to 51K. Larger values favor lower duty cycles. Using the maximum value of 51K for the published values and solving for C3 we obtain:

² The multiplication factor 1.17 is estimated based on measured data.

$$C3 \approx 401.3\mu\text{s} / (0.69 * 51\text{K}) \approx 11.4\text{nF}.$$

The on time may be expressed in terms of the off time:

$$\text{Equation 3: } \text{On time} \approx 1.68 * (R1 + R5 + R3) / (R2 + R4) * \text{Off time} + 1.17 * (R1 + R5) * C4$$

Minimum duty cycle occurs when C4 is omitted entirely. Without the second timing filter pole, on time to off time ratio simplifies to the ratio of the total resistance in each section. Given a target duty cycle of 3.7% we obtain:

$$\text{Equation 4: } (R1 + R5 + R3) \approx (R2 + R4) * \text{On time} / \text{Off time}$$

$$(R1 + R5 + R3) \approx 51\text{k} * 15.4\mu\text{s} / 401.3\mu\text{s} \approx 1.96\text{K}$$

R5 alone is 5.1K, and R3 is 1K. The predicted minimum duty cycle without changing R5 and R3 is then:

$$\text{Equation 5: } \text{Duty cycle min} \approx 6.1\text{K} / (51\text{K} + 6.1\text{K}) \approx 10.6\%$$

Additional changes are therefore required to reach the targeted on time and duty cycle. The intended duty cycle may be obtained by replacing R5 with a 1K Ohm resistor, shorting R3, and adjusting R1 almost to zero. This requires four component changes to the circuit: Remove C4, change C3 from 3.3nF to 10nF, replace R5 with 1K Ohm and replace R3 with a short. Figure 7 depicts the resulting circuit. Figure 8 shows an oscilloscope capture using the modified circuit with R1 and R2 adjusted to obtain the reported frequency and duty cycle values.

Simple mistakes such as component value transcription or transposition of components cannot account for such extensive circuit modifications. This author concludes that the authors either did not use a circuit resembling what they published, or that they did not obtain the operating frequency and duty cycle that they reported.

A very likely explanation is that the authors transposed on and off times when calculating their duty cycles. The complementary duty cycle to 3.7% is 96.3%. A 96.3% on duty cycle at 2.4kHz requires a 401.3us on time and a 15.4us off time. Table 2 shows that with the potentiometers R1 and R2 both centered, the on time is 563us and the off time is 13.4us. Table 2 further shows that on time may be adjusted as low as 303us, and that off time may be adjusted as high as 116us. Figure 9, shows an oscilloscope capture obtained using the published schematic (with typographical error on R5 corrected), where R1 and R2 have been adjusted to obtain 2.4kHz and 96.3% duty cycle operation without any change in: component values, or circuit wiring.

Because the complement duty cycle is readily attainable with the published circuit and the reported duty cycle cannot be obtained from either the published circuit or minor

corrections to the published circuit, this author concludes that the authors erroneously reported the complement instead of the true on duty cycle.

That error suggests that the authors also calculated input power based on the erroneous 3.7% duty cycle instead of the actual 96.3% duty cycle. This would result in under reporting input power by: $96.3/3.7$, IE 26:1. A 26:1 error factor greatly exceeds the authors' claimed energy gain of 16:1.

Summary and Conclusions

This author has shown that the published control circuit in: "Transient energy enhances energy co-efficients" by R A Ainslie and B C Buckley does not produce the waveform timing cited by the authors. This author has further shown that the claimed waveform duty cycle and frequency may not be obtained by simple substitution of one or two component values, nor by transposition of components. This author has further shown that the complement duty cycle at the claimed operating frequency is easily obtained with the circuit form and populated values reported by the authors. This author therefore concludes that the authors confused on duty cycle for its complement.

The use of the complement rather than the true duty cycle is a serious error that potentially upsets the experiment power balance by a factor of 26:1. That factor is greatly in excess of the claimed circuit average power gain. Therefore, barring further corroborating evidence, the findings and conclusions offered by the authors Ainslie and Buckley in the subject paper are shown to be based on serious errors and must be rejected. The authors are encouraged to either: produce corroborating evidence and make appropriate corrections to their paper, or to retract their claims.

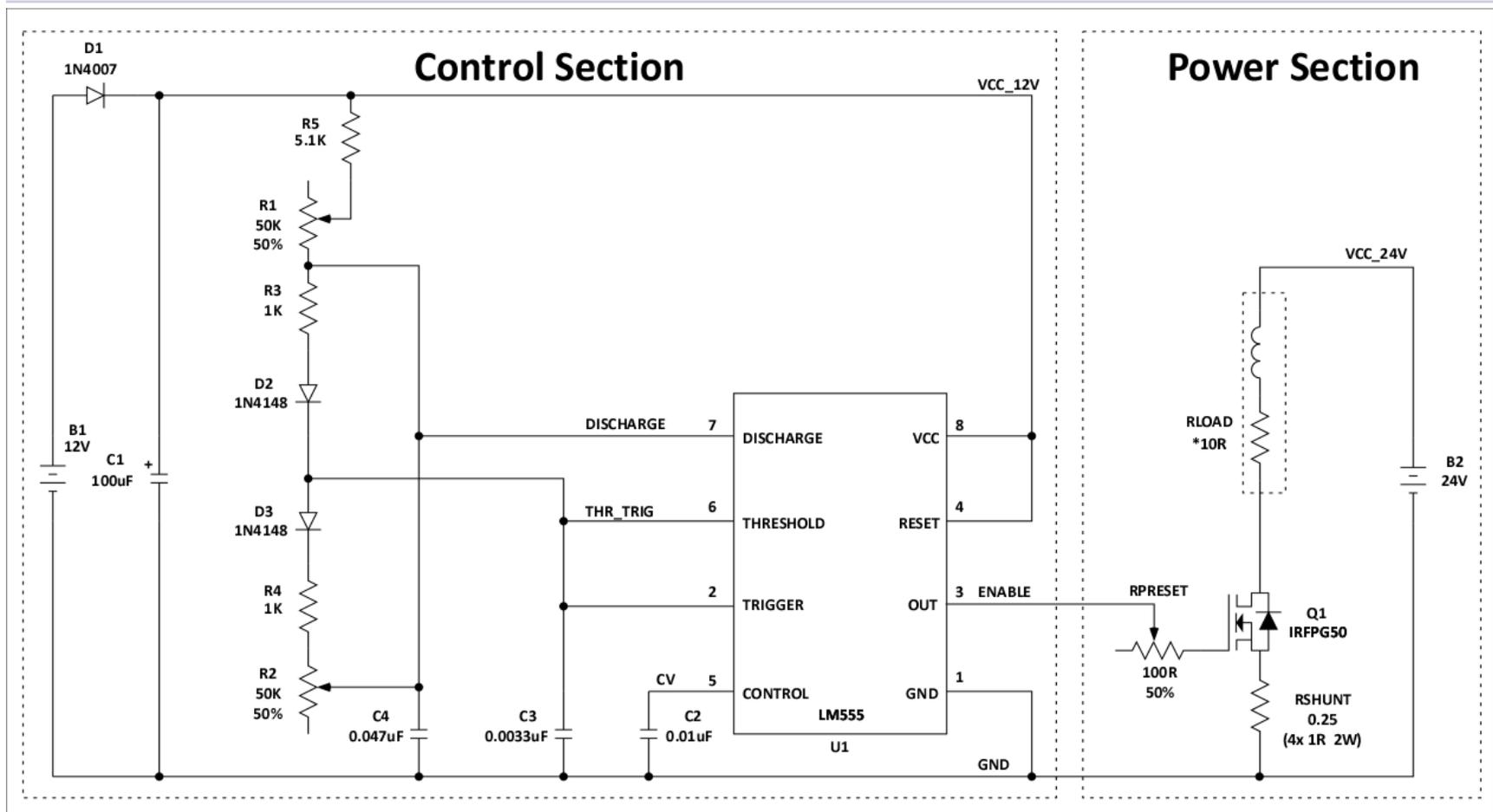


Figure 4, 'Quantum' 2002 Circuit (R5 corrected from 5.2K typographical error)

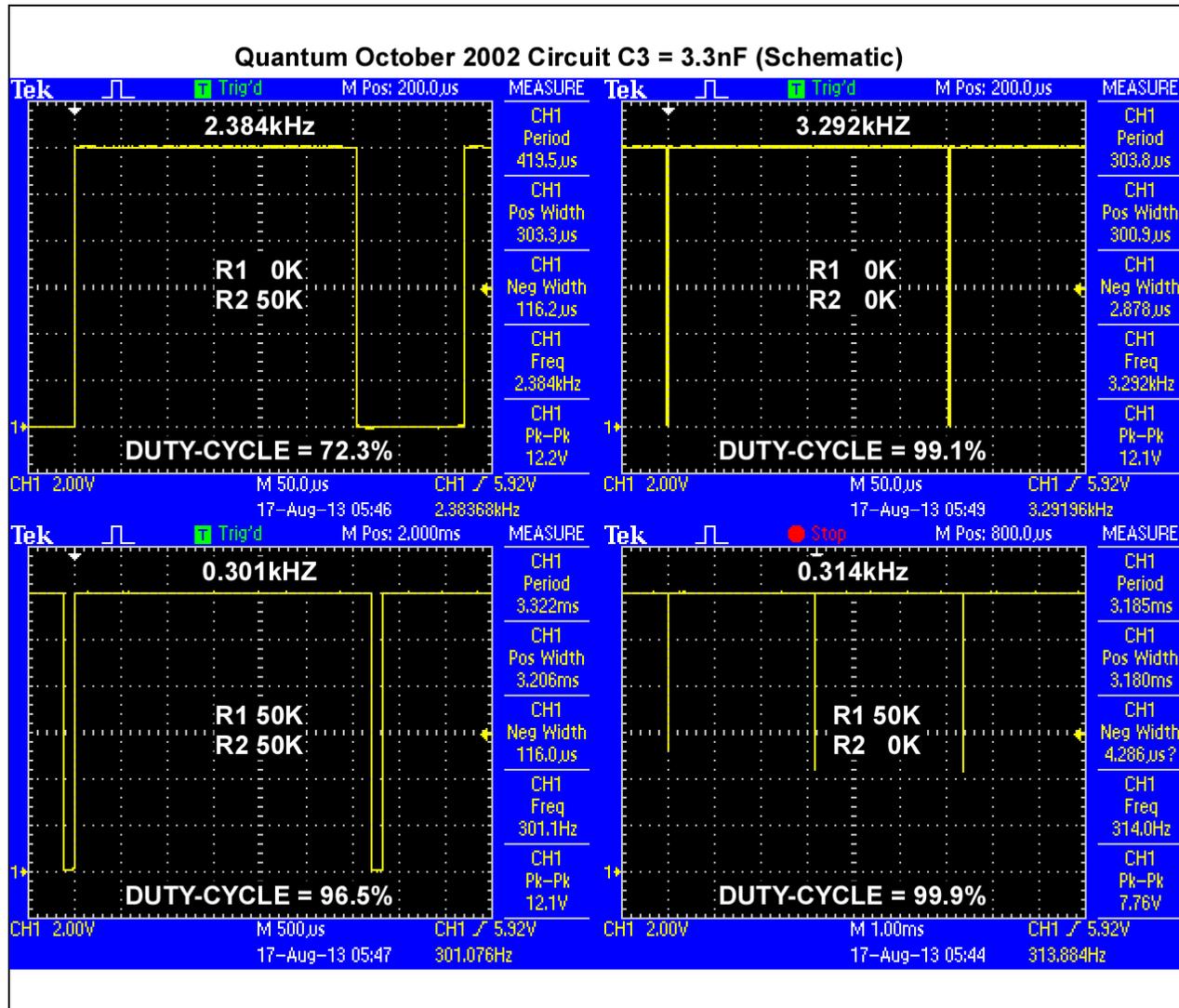


Figure 5, Measured Timing Range, 'Quantum' Magazine Circuit C3 = 3.3nF

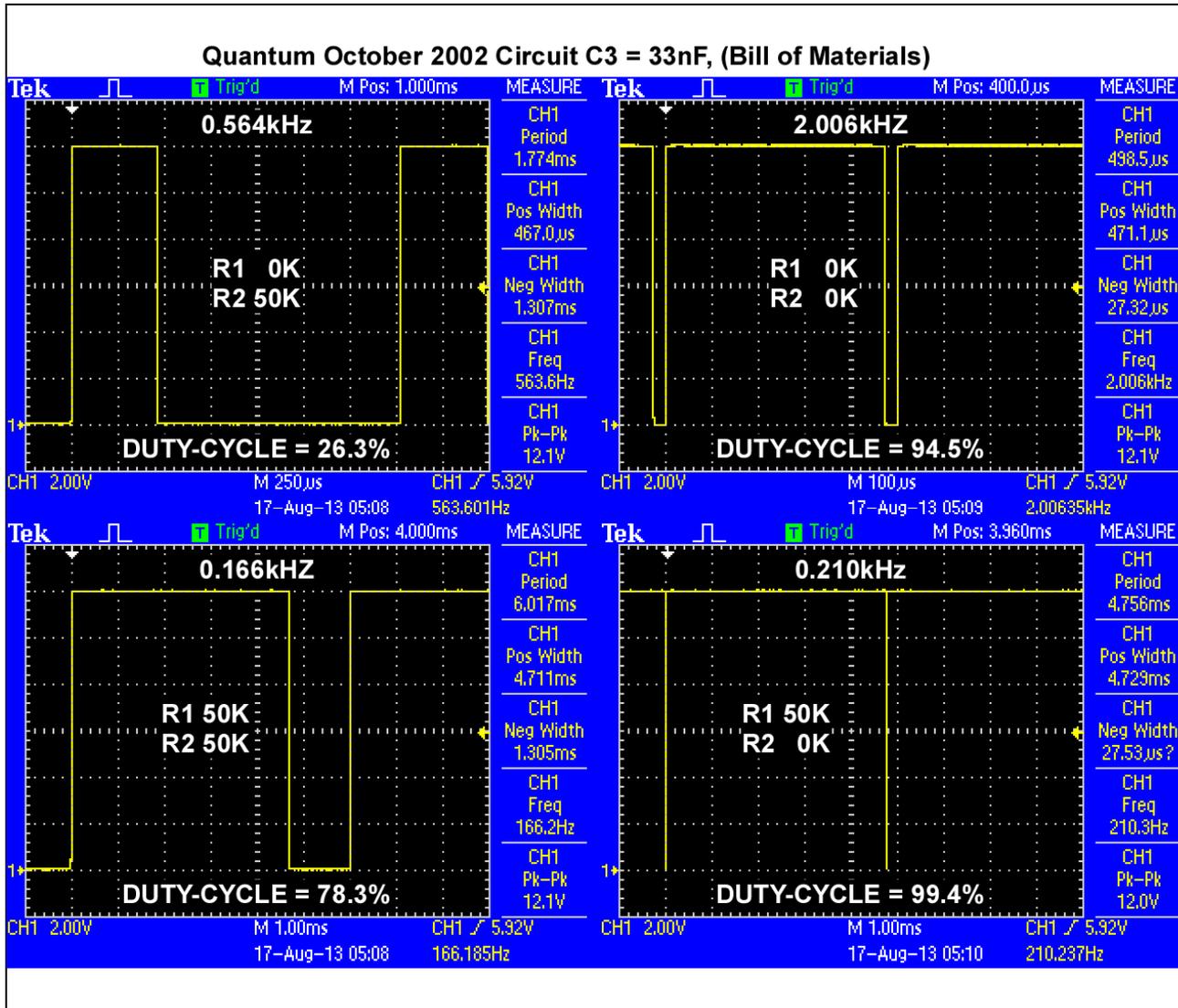


Figure 6, Measured Timing Range, 'Quantum' Magazine Circuit C3 = 33nF

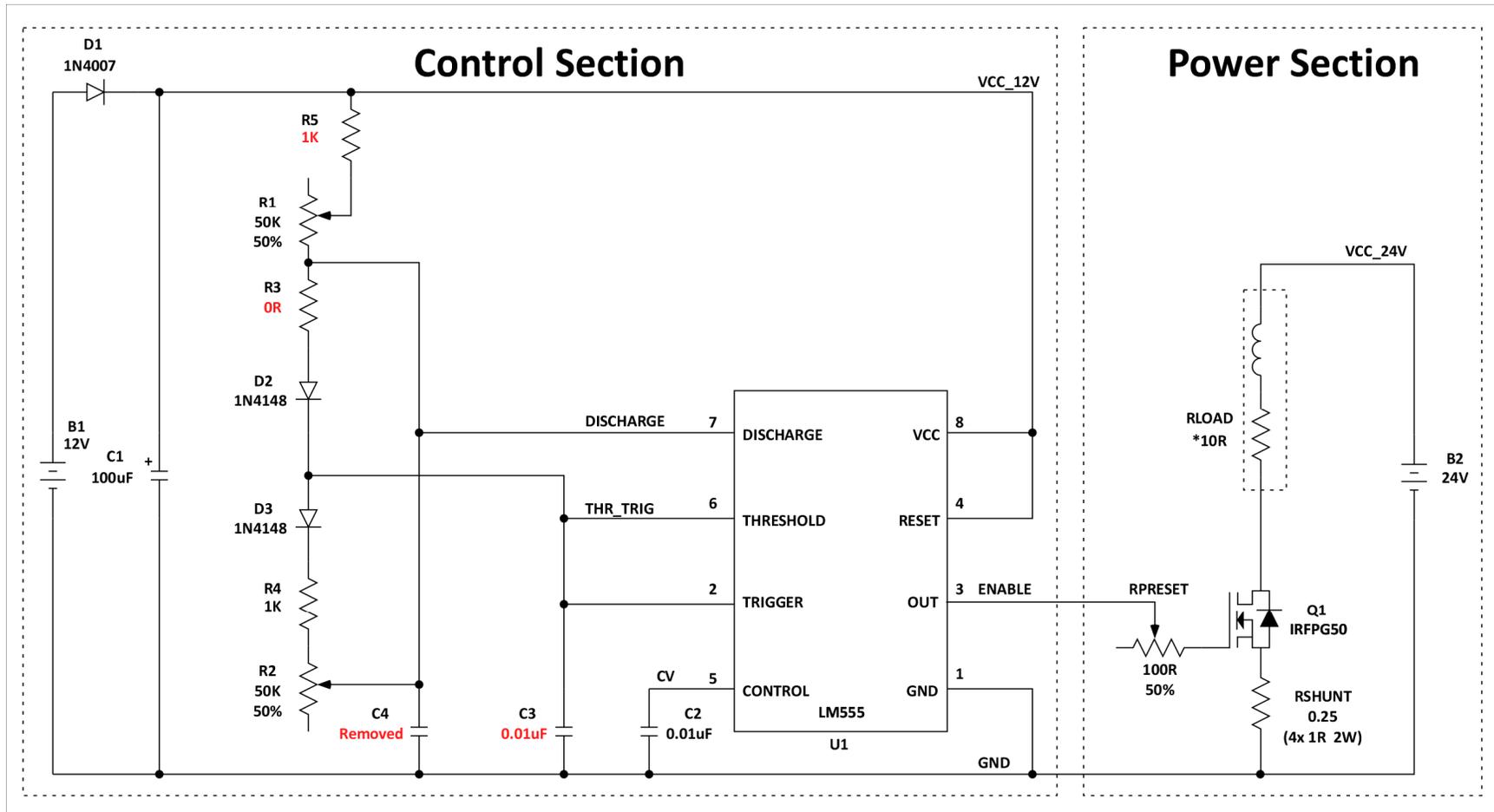


Figure 7, Component Changes Substitutions for 3.7% Duty Cycle 2.4kHz

**Quantum 2002 Circuit Modified:
C4 Removed, C3 = 10nF,
R5 = 1K, R3 = 0R**

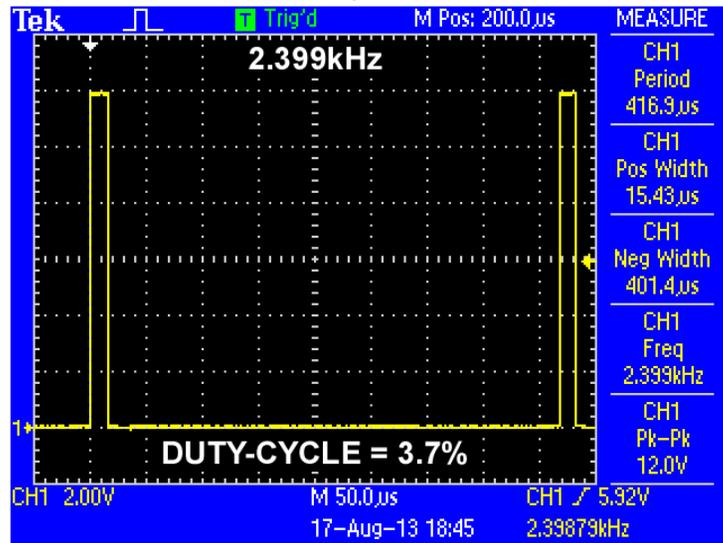


Figure 8, Modified Circuit Performance

**Quantum 2002 Circuit
R1, R2 Adjusted for
2.4kHz, 96.3% Duty Cycle**

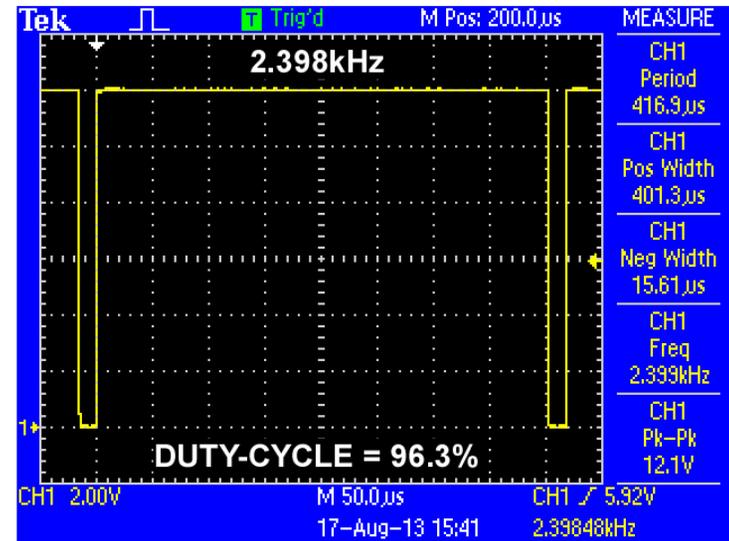


Figure 9, 'Quantum' Circuit Adjusted to 2.4kHz, 96.3% Duty Cycle

ADDENDUM 1 8/24/2013

The 'Quantum' magazine author: Ms. Rosemary Ainslie has issued strenuous objections to this author expressing in essence that neither the control circuit nor its timing is a significant element of the 'Quantum' magazine article:

"The fact that there may or may not be a mix up in the design of the 555 switching circuit is IMMATERIAL. I have questioned our academics on this and have been advised that the timing circuit has NOTHING to do with the claim - therefore it does NOT require amendment. In fact the timing circuit should, correctly, have been omitted from that circuit. Nor can I comment on whether there's an error there or not. I did not do that design. I'm not capable of doing it. But I will say this. The circuit was accredited - under operating conditions, by SASOL South Africa - BP South Africa - ABB Research in North Carolina - SPESCOM - ALSTOM and MANY other smaller and unlisted companies. They all have their own engineering experts. And ALL of them confirmed these results. AND they then went further by actually accrediting those results."³

The difficulty with the position taken by Ms. Ainslie is that the remainder of the circuit is an extremely common circuit construct known as a low side driver. This construct has been used for many decades in everything from: electric toothbrushes to cellular telephones, without any reports of the excess energy claimed in the 'Quantum' article. It is therefore incumbent upon the authors to stipulate at least one specific set of circumstances under which the novel behavior they claim has been observed and may be observed by others.

The 'Quantum' article stipulates an exciting waveform: 2.4kHz at 3.7% duty cycle delivered from an LM555 through a 100 Ohm variable resistor as one such waveform. However, the apparatus documented in the 'Quantum' magazine article cannot produce such a waveform. This is a fact that this author recently discovered was acknowledged by Ms. Ainslie herself on August 9th 2009:

"Thanks for the video Aaron. Yet again, it seems that I need to apologise. The published circuit clearly does not cut it and TK's complaints about the design appear to be valid.

So - let me again apologise to TK. Abject apologies about this. It does seem that the circuit design was erroneous and your comments regarding this were valid. I should, indeed, have had the circuit checked before publication.

And apologies to all those who built that circuit. The only thing that I can assure you is that the design is erroneous - not our test results. Hopefully Aaron can tweek the circuit to get the duty cycle function up to par - and yet hold onto that oscillation. It's just so much in line with our own findings here.

Sorry TK. Abject apologies. But run with that 'wrong' switch. It should, at its least, give the required waveform oscillations."⁴

This author has invited Ms. Ainslie to produce any documentation that she might have of corroboration she obtained from any third party. Ms. Ainslie has not produced any.

³ The full text is available at: <http://www.energy-shiftingparadigms.com/index.php/topic,2313.msg4903/topicseen.html#msg4903>

⁴ <http://www.energeticforum.com/inductive-resistor/4314-cop-17-heater-rosemary-ainslie-63.html>

Addendum 2 8/27/2013

8/27/2013 Rosemary Ainslie published a schematic of the “Demo Kit 1” that she represents was used to collect data for the subject October 2002 ‘Quantum’ magazine article. The schematic was produced by Steve Weir by reverse engineering from photographs taken of the apparatus. Ms. Ainslie has posted the photographs to her forum. Members of her forum can view the photographs there.

<http://www.energy-shiftingparadigms.com/index.php/topic,2313.msg4937.html#msg4937>

The reverse engineered schematic appears at:

<http://www.energy-shiftingparadigms.com/index.php/topic,2313.msg4949.html#msg4949>

This author has redrawn the schematic in the closest possible form to Figure 4, as Figure 10 below. About the only thing in common between the two circuits is the use of a 555 timing IC and an N channel MOSFET switch. The particular 555 used is an NE555 manufactured by ST Microelectronics.

The “Demo Kit 1” apparatus employs 1N4007 power rectifiers in place of the 1N4148A signal diodes as shown in the article schematic as the steering diodes of the 555 timing network. The leakage current of a 1N4007 is on the order of 5uA, two hundred times greater than the leakage current of a 1N4148A is on the order of 25nA. This has a small impact on the output high time, but a major impact on the output low period of the circuit.

The output high interval is set by the 330 Ohm pull-up resistor R3 and the timing capacitor C3. The series combination: R4, R2, and D2 appear in parallel with D3 and slightly increase C3 charging current, shortening the on period which would nominally be:

Equation 6: $T_{on} = -\ln(3.4/7.4) * 330 * 1.5E-9 = 384ns.$

Actual on time extends due to the internal circuit response time of the 555.

Off times would normally range from:

Equation 7: $T_{off} = -\ln(3.4/7.4) * \{6800 - 56,800\} * 1.5E-9 = 7.9us - 66us.$

However, reverse leakage through D3 greatly reduces the periods to between: 1.2us and 8.0us as seen in Figure 11. Here, we can see that the duty-cycle is getting close to what was reported in the ‘Quantum’ article, but that the operating frequency is off by two orders of magnitude.

As a cross check the timing circuit was reconfigured with 1N4148A signal diodes and retested. The results appear in Figure 12. On times ranged from 477ns to 487ns, 24% to 27% greater than the equations predict. Off times ranged from 9.3us to 74.5us, 13% to 17% greater than the equations predict. Overall the performance is within reasonable expectations. The greater percentage variation between predicted and measured performance corresponds to shorter periods. 13% of the variation is attributable to component value tolerances. The remaining variation is attributable to the response delays of the TLC555 circuit. These delays will be worse with the NE555 used by Ms. Ainslie and so on times should be expected to increase by 100ns – 200ns.

Rather than reconcile the questions raised by the contradiction between the stimulus specified in the article and the circuit specified by the article, Ms. Ainslie now presents an entirely different circuit that generates entirely different waveform timing and other important differences.

The “Demo Kit 1” does not include the variable resistor between the 555 output and the N MOSFET gate depicted in the ‘Quantum’ article. Further, the N MOSFET type is an IRFP450 with 25% lower total gate charge than the IRFPG50 stipulated in the ‘Quantum’ article.

A potentially very important difference is that the circuit common of the “Demo Kit 1” is at the source of Q1, whereas it is at the negative battery terminal in the ‘Quantum’ magazine article. Oscilloscope measurements across shunt resistors connected in the “Demo Kit 1” will read negative values when the battery is supplying current, whereas under the same conditions they will read positive values in the ‘Quantum’ magazine article configuration.

Finally, the circuit connects the current sense resistors through banana terminal jacks. The length of patch wires used between those jacks will have a major impact on the parasitic inductance between the circuit common at the source pin of Q1 and the bodies of the current sense resistors. The subject article does not specify those lead lengths.

Ms. Ainslie’s August 11 demonstration well illustrates the power measurement corruption that can occur when high frequency currents traverse inductive interconnects between a voltage source such as a battery and the voltage sense and current sense resistor and the associated voltage sense. The use of: ordinary 2W resistors for current sense, connected through banana jacks with external patch cables, and patch cables to the battery pack means that there is every reason to expect that the same stray inductance based errors that poisoned the “Q Array” measurements as demonstrated August 11 corrupted any and all measurements taken on the “Demo Kit 1” fixture.

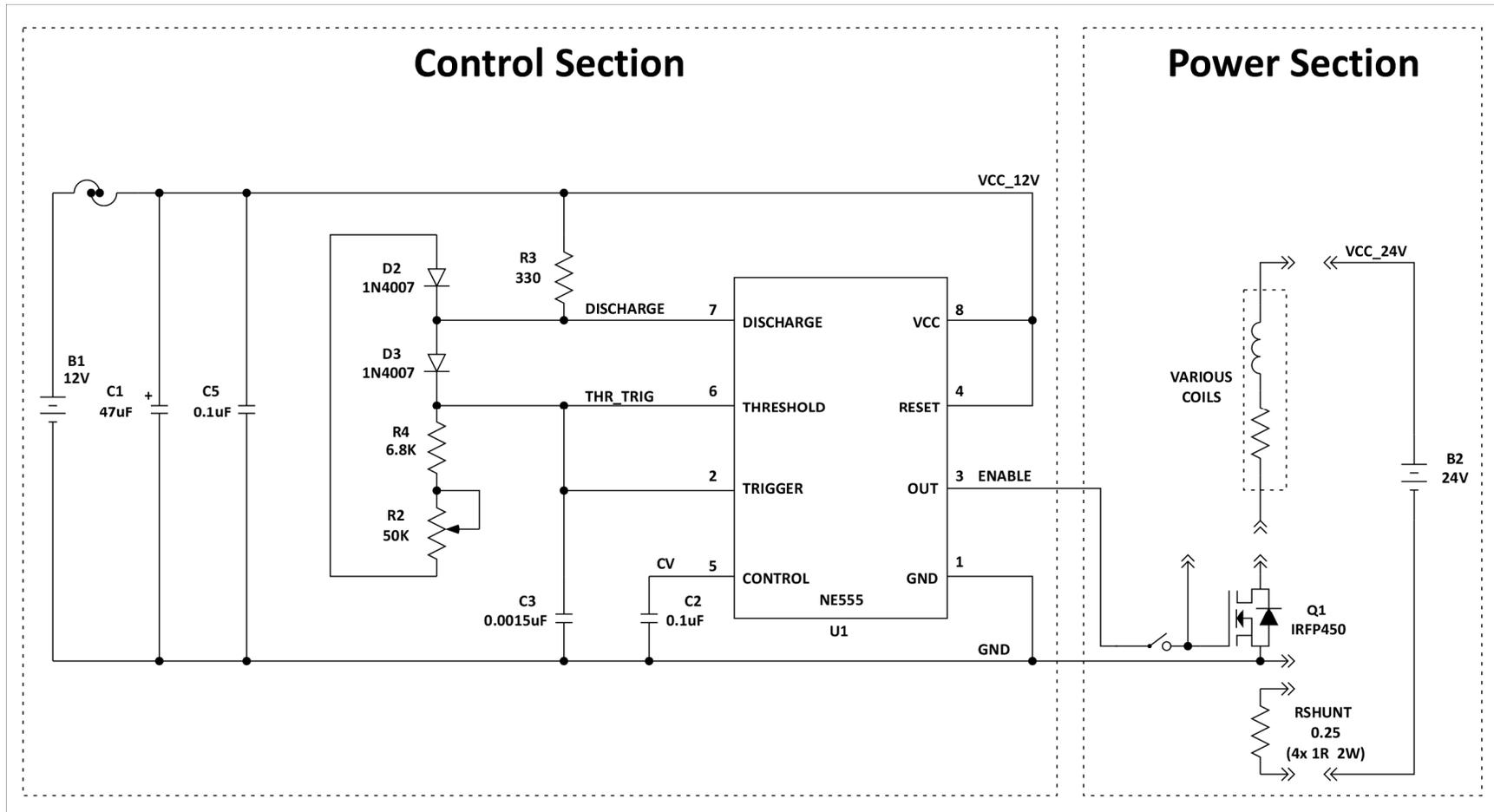


Figure 10, "Demo Kit 1" Schematic Redrawn from Reverse Engineered Schematic Produced by Steve Weir

"DEMO KIT 1" Measured Performance

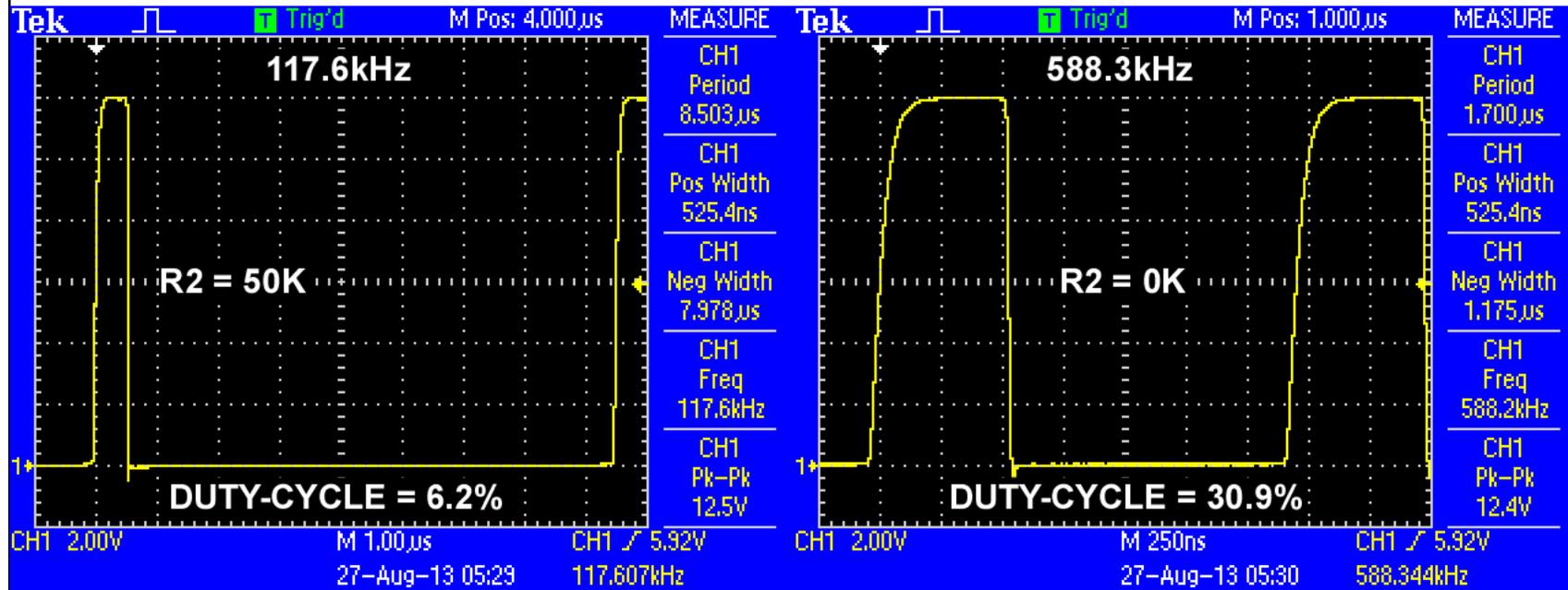


Figure 11, "Demo Kit 1" Measured Performance

“DEMO KIT 1” Measured Performance 1N4148A Diodes

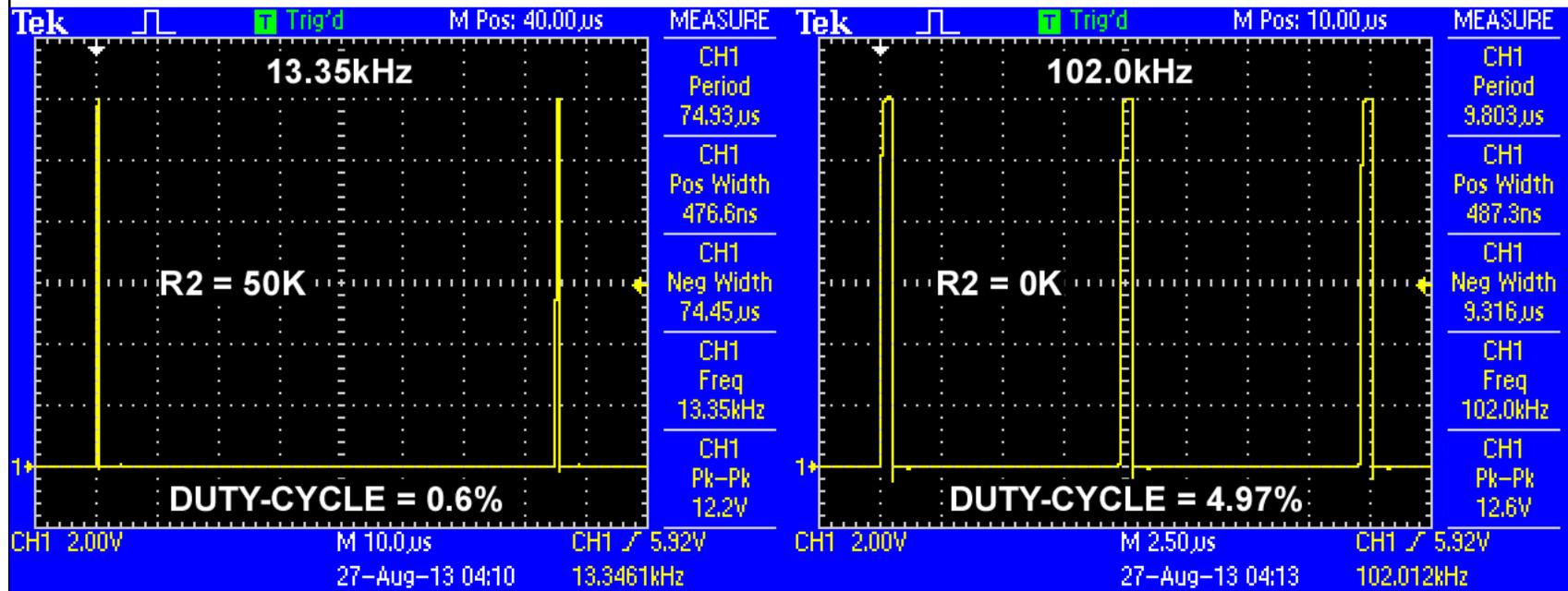


Figure 12, "Demo Kit 1" Substituting 1N4148A Diodes for 1N4007 Diodes Used

Revisions

8/24/2013 Changed instances of Quantum to 'Quantum'. Corrected C3 value in Figure 7. Added Addendum 1.

8/27/2013 Added Addendum 2.